

# Zilog

Z08430 Customer  
Procurement Spec (CPS)

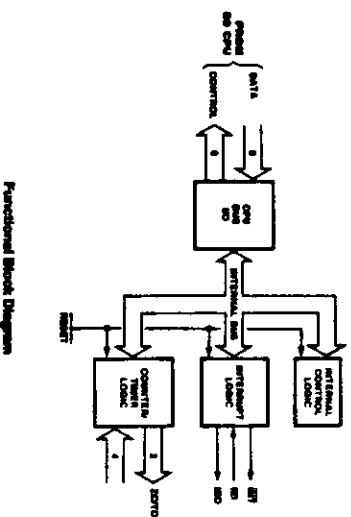
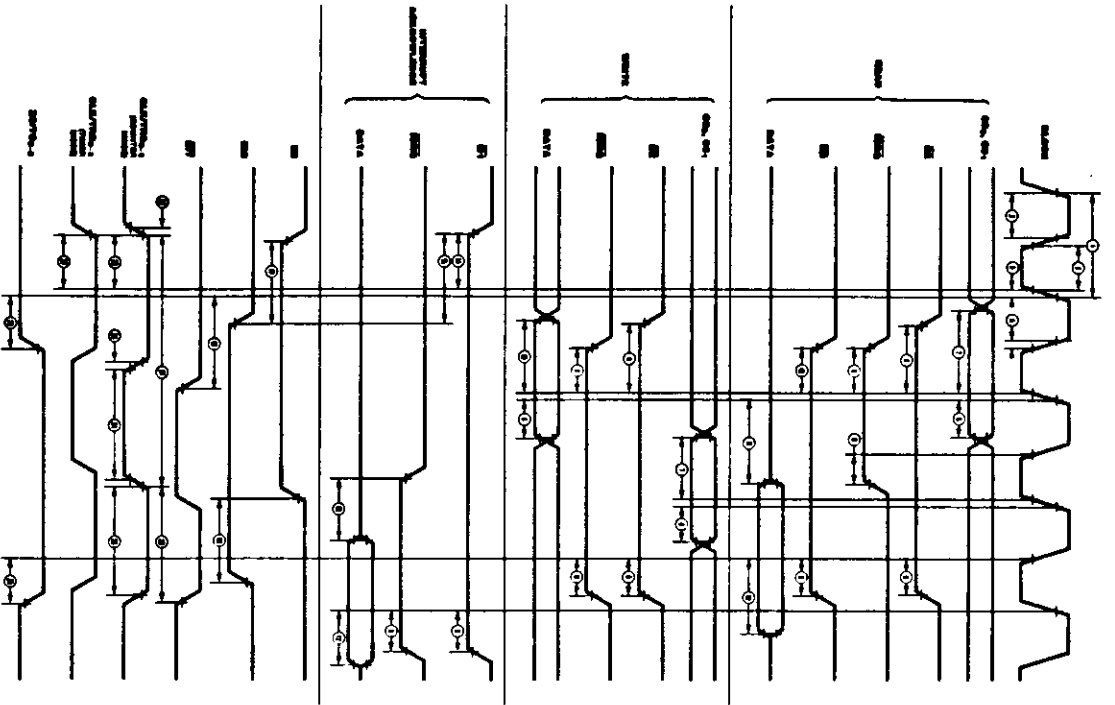
## GENERAL DESCRIPTION

The Z80 CTC four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SID with no additional logic. In larger systems, address decoders and buffers may be required.

Programming the CTC is straightforward: each channel is programmed with two bytes; a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified; the CTC internally generates a unique vector for each channel.

The Z80 CTC requires a single +5V power supply and the standard Z80 single-phase system clock. It is fabricated with n-channel silicon-gate depletion-load technology and packaged in a 28-pin and a 44-pin chip carrier DIP.

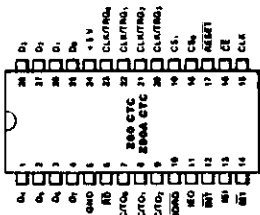


Functional Block Diagram

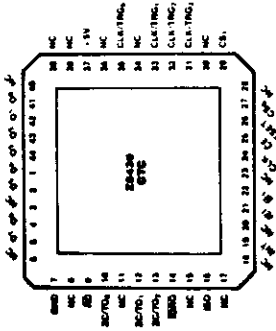
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**AC CHARACTERISTICS**



**48-pin Dual-In-Line Package (DIP)  
Pin Assignments**



**44-pin Quad Flat Pack, Pin Assignments**

**DC CHARACTERISTICS**

Symbol	Parameter	Min	Max	Unit	Condition
V <sub>IL</sub>	Check Input Low Voltage	-0.3*	+0.45*	V	V <sub>CC</sub> = 2.0 mA
V <sub>IOH</sub>	Check Input High Voltage	V <sub>CC</sub> - 0.3*	V <sub>CC</sub> + 0.3*	V	I <sub>OH</sub> = -250 μA
V <sub>IL</sub>	Input Low Voltage	-0.3*	+0.3*	V	
V <sub>IH</sub>	Input High Voltage	V <sub>CC</sub> - 0.3*	V <sub>CC</sub> + 0.3*	V	
V <sub>OL</sub>	Output Low Voltage	+0.05	+0.45	V	
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> - 0.3	V <sub>CC</sub> + 0.3	V	
I <sub>CC</sub>	Power Supply Current		+120*	μA	V <sub>IN</sub> = 0.4 to V <sub>CC</sub>
I <sub>L</sub>	Input Leakage Current		± 10*	μA	V <sub>OH</sub> = 1.5 V
I <sub>OD</sub>	3-State Output Leakage Current in High		± 10*	μA	V <sub>OH</sub> = 1.5 V
I <sub>OD</sub>	3-State Output Leakage Current in Low		-1.0*	μA	V <sub>OH</sub> = 1.5 V

\* Tested  
 † Guaranteed by Design  
 ‡ Guaranteed by Characterization

Number	Symbol	Parameter	20M CTC		25M CTC		30M CTC	
			Min	Max	Min	Max	Min	Max
1	T <sub>0C</sub>	Clock Cycle Time	400	(1)	250	(1)	165	(1)
2	T <sub>0Ch</sub>	Clock Width (High)	170	2000	105	2000	65	2000
3	T <sub>0Cl</sub>	Clock Width (Low)	170	2000	105	2000	65	2000
4	T <sub>0Cf</sub>	Clock Fall Time	30	30	30	30	20	20
5	T <sub>0Cr</sub>	Clock Rise Time	30	30	30	30	20	20
6	T <sub>0H</sub>	All Hold Times	0	0	0	0	0	0
7	T <sub>0SC</sub>	CS to Clock Setup Time	160	160	100	100	100	100
8	T <sub>0EC</sub>	CE to Clock Setup Time	200	200	150	150	100	100
9	T <sub>0DC</sub>	RD/WR to Clock Setup Time	250	250	115	115	70	70
10	T <sub>0DCl</sub>	RD to Clock Setup Time	240	240	200	200	130	(2)
11	T <sub>0DCl</sub>	RD to Data Out Delay						
12	T <sub>0DCl</sub>	RD to Data Out Delay						
13	T <sub>0DCl</sub>	RD to Data Out Delay						
14	T <sub>0DCl</sub>	RD to Data Out Delay						
15	T <sub>0DCl</sub>	RD to Data Out Delay						
16	T <sub>0DCl</sub>	RD to Data Out Delay						
17	T <sub>0DCl</sub>	RD to Data Out Delay						
18	T <sub>0DCl</sub>	RD to Data Out Delay						
19	T <sub>0DCl</sub>	RD to Data Out Delay						
20	T <sub>0DCl</sub>	RD to Data Out Delay						
21	T <sub>0DCl</sub>	RD to Data Out Delay						
22	T <sub>0DCl</sub>	RD to Data Out Delay						
23	T <sub>0DCl</sub>	RD to Data Out Delay						
24	T <sub>0DCl</sub>	RD to Data Out Delay						
25	T <sub>0DCl</sub>	RD to Data Out Delay						
26	T <sub>0DCl</sub>	RD to Data Out Delay						
27	T <sub>0DCl</sub>	RD to Data Out Delay						
28	T <sub>0DCl</sub>	RD to Data Out Delay						
29	T <sub>0DCl</sub>	RD to Data Out Delay						
30	T <sub>0DCl</sub>	RD to Data Out Delay						
31	T <sub>0DCl</sub>	RD to Data Out Delay						
32	T <sub>0DCl</sub>	RD to Data Out Delay						
33	T <sub>0DCl</sub>	RD to Data Out Delay						
34	T <sub>0DCl</sub>	RD to Data Out Delay						
35	T <sub>0DCl</sub>	RD to Data Out Delay						
36	T <sub>0DCl</sub>	RD to Data Out Delay						
37	T <sub>0DCl</sub>	RD to Data Out Delay						
38	T <sub>0DCl</sub>	RD to Data Out Delay						
39	T <sub>0DCl</sub>	RD to Data Out Delay						
40	T <sub>0DCl</sub>	RD to Data Out Delay						
41	T <sub>0DCl</sub>	RD to Data Out Delay						
42	T <sub>0DCl</sub>	RD to Data Out Delay						
43	T <sub>0DCl</sub>	RD to Data Out Delay						
44	T <sub>0DCl</sub>	RD to Data Out Delay						
45	T <sub>0DCl</sub>	RD to Data Out Delay						
46	T <sub>0DCl</sub>	RD to Data Out Delay						
47	T <sub>0DCl</sub>	RD to Data Out Delay						
48	T <sub>0DCl</sub>	RD to Data Out Delay						

(1) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (2) Increase delay by 10 ns for each 50 pF increase in loading, 200 pF maximum for data lines and 100 pF for control lines  
 (3) Increase delay by 2 ns for each 10 pF increase in loading, 100 pF maximum  
 (4) Tri-state mode  
 (5) Counter mode  
 (6) Penultimate numbers reference the data number of a parameter  
 (7) (1) refers to T<sub>0C</sub>  
 (8) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (9) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (10) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (11) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (12) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (13) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (14) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (15) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (16) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (17) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (18) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (19) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (20) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (21) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (22) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (23) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (24) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (25) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (26) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (27) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (28) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (29) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (30) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (31) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (32) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (33) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (34) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (35) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (36) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (37) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (38) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (39) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
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 (43) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (44) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (45) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (46) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (47) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>  
 (48) T<sub>0C</sub> = T<sub>0Ch</sub> + T<sub>0Cl</sub> + T<sub>0Cf</sub>

\* Clock-cycle time-dependent characteristics. See footnotes to AC Characteristics.  
 † Loadings are preliminary and subject to change. Units in parentheses.  
 ‡ Guaranteed by Design  
 § Guaranteed by Characterization